

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)	
)	
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MARK L. DOCZY)	
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MATTHEW V. METZ)	
JACK KAVALIEROS)	
ROBERT S. CHAU)	
)	Art Unit: unknown
Serial No.: unknown)	
)	Examiner: unknown
Filed: unknown)	
)	Attorney Docket: P17280
For: A METHOD FOR MAKING)	
A SEMICONDUCTOR)	
DEVICE HAVING A HIGH-K)	
<u>GATE DIELECTRIC</u>)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is being submitted under 37 C.F.R. §1.97(b). Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the references cited on that form. It is respectfully requested that the cited references be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made

and is not to be construed as an admission that the information cited in this statement constitutes prior art or is otherwise material to patentability.

Respectfully submitted,

Dated: August 26, 2003 Mark V. Seeley
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August 28, 2003
(Date signed)

Form PTO-1449 (Modified)		Atty Docket No.: 42P17280		Serial No.: Unknown			
List of Patents and Publications Statement (Use several sheets if necessary)				Applicant: Justin K. Brask et al.			
				Filing Date: Herewith			
REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS				
Examiner Initials		Document No.		Class	Sub- Class	Filing date if appropriate	
	AA	5,625,217	Chau et al.	257	412		
	AB	5,753,560	Hong et al.	438	402		
	AC	5,783,478	Chau et al.	438	592		
	AD	5,891,798	Doyle et al.	438	624		
	AE	6,063,698	Tseng et al.	438	585		
	AF	6,087,261	Nishikawa et al.	438	685		
	AG	6,184,072	Kaushik et al.	438	197		
	AF	6,306,742 B1	Doyle et al.	438	591		
	AI	6,391,802 B1	Delpech et al.	438	785		
	AJ	6,420,279	Ono et al.	48	785		
	AK	6,475,874	Xiang et al.	438	396		
	AL	6,544,906	Rotondaro et al.	438	785		
	AM	US2003/032303	Yu et al.	438	770		
FOREIGN PATENT DOCUMENTS							
		Document No.	Date	Country	Class	Sub-Class	Translation
	AM						
	AN						
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)							
	AO	Doug Barlage et al., "High-Frequency Response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics", 2001 IEEE, 4 pages.					
	AP	Robert Chau et al., "A 50nm Depleted-Substrate CMOS Transistor (DST), 2001 IEEE, 4 pages.					
	AQ	Lu et al., "Dual-Metal Gate Technology for Deep-Submicron CMOS Devices", dated April 29, 2003, 1 page.					
	AR	Schwantes et al., "Performance Improvement of Metal Gate CMOS Technologies with Gigabit Feature Sizes", Technical University of Hamburg-Harburg, 5 pages.					
	AS	Chau et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/082,530, Filed February 22, 2002					
	AT	Parker et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/285,915, Filed October 31, 2002					
	AU	Chau et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/288,043, Filed November 5, 2002					
	AV	Parker et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/315,268, Filed December 10, 2002					
	AW	Doczy et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/338,174, Filed January 7, 2003					
	AX	Brask et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/387,303, Filed March 11, 2003					
	AY	Brask et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/391,816, Filed March 18, 2003					
	AZ	Chau et al., "A Method for Making a Semiconductor Device Having a Metal Gate Electrode", Serial No. 10/431,166, Filed May 6, 2003					
	BA	Brask, et al, "A Method for Making a Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/441,616, filed May 20, 2003					
Examiner			Date Considered				

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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